UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,637	06/30/2000	Jin Yang	42390.P9429	9275

8791 7590 09/21/2007

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

MAIL DATE	DELIVERY MODE
09/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/608,637
Filing Date: June 30, 2000
Appellant(s): YANG, JIN

Lawrence M. Mennemeier
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/11/2007 appealing from the Office action mailed 12/7/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: Claims 4-5, 8, 14-18, 28 and 31-40 are not being rejected for lacking utility under 35 U.S.C. 101, they are being rejected under 35 U.S.C. 101 for being directed towards non-statutory subject matter.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 4, 5, 8, 14-18, 28 and 31-40 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

35 U.S.C. § 101 requires that an Applicant's invention disclose a *useful, tangible and concrete* result.

Claims 4, 5, 8, 14-18, 28 and 31-40 fail to disclose a tangible, concrete and useful result, although Applicant's specification discloses *automated design verification for large scale integrated circuits* the specification also discloses that the *verification* can be for *other finite state systems,* the current claim language teaches *verification of other finite state system,* as such the current claim language, even in light of Applicant's specification, fails to disclose a useful result because there is no disclosure in either the claim language or the specification as to what the *other finite state system* would be. Further, the currently claimed limitation of *other finite system* is not tied to the actual physical world, for example, a *finite system* could be a finite state machine, which is an abstract concept and does not affect the physical world because it is a theoretical construct.

Claims 4, 5, 8, 14-18, 28 and 31-40 fail to disclose a useful concrete and tangible result. The current claim language discloses, initializing a structure and checking a structure for

verifying properties expressed as assertion graph instances however, the current claim language fails to disclose any link to the physical world, manipulation of a assertion graph on a plurality of symbolic lattice domains fails to disclose or suggest any resultant output linking the verification of the circuit to the physical world. Applicant's instant amendments fail to disclose that any verification result is being presented into the real world. The current claim language fails to disclose providing a display of the resultant verification to a user as well as providing any signal or file to affect the production of the actual integrated circuit. Further, the manipulation of an assertion graph and the subsequent verification of a symbolic simulation relation is merely teaching the manipulation of an abstract concept, which is non-statutory subject matter, see section 2106.02 of the Rev. 5 Aug. 2006 revision of the MPEP.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 5, 8, 14-18, 28 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, 5, 8, 14-18, 28 and 31-40 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: how *a formal verification of a circuit* is performed by *initialization of a symbolic simulation relation for an assertion graph on*

a first lattice domain. The current claim language fails to provide a linkage between *circuit verification* and manipulation/initialization of an *assertion graph in a first symbolic lattice domain*.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. The rejection of claim 28 for being directed to non-statutory subject matter because *means for initializing, means for computing* and *means for checking* have been argued to include a computing system, and not merely software modules and therefore that aspect of the 35 U.S.C. 101 rejection of claim 28, as being directed to software, has been withdrawn.

Claims 4, 5, 8,14-18, 28 and 31-40 rejected under 35 U.S.C. 112 second paragraph for lack of clarity regarding the instant limitation, *other finite state system*. Appellant's have clearly defined the meaning of this term in the arguments set forth and therefore this rejection is withdrawn.

(10) Response to Argument

Regarding the arguments Appellants' submitted on page 11-13 of the Appeal Brief regarding the 35 U.S.C. 112 rejections of claims 4, 5, 14-18, 28 and 31-40 Appellant's argued;

> The issue of definiteness is whether, in light of the teachings of the prior art and of the particular invention, the claims set out and circumscribe a particular area with a reasonable degree of precision and particularity. *In re Moore*, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971).
>
> With regard to whether the instant claim provides linkage between circuit verification and manipulation/initialization of a symbolic simulation relation for an assertion graph in a first symbolic lattice domain, appellant respectfully submits that claim 1 sets forth that the assertion graph on the first symbolic lattice domain is configurable to express a justification property to verify by computing the symbolic

simulation relation. Thus the instant claim clearly does provide linkage between circuit verification and manipulation/initialization of a symbolic simulation relation for an assertion graph in a first symbolic lattice domain.

The test for definiteness under 35 U.S.C § 112 is whether those skilled in the art would understand what is claimed when the claim is read in light of the specification. Orthokinetics, Inc. v. Safety Travel Chairs, Inc., 806 F2d 1565, 1576, 1USPQ2d, 1081, 1088 (Fed. Cir. 1986).

It will be appreciated that there is a direct correspondence between the formal definition of Sims(e) and the initialization performed by Box 311 of Figure 3a. Appellant respectfully submits that at least in light of the above disclosure set forth by the specification, the claims set out and circumscribe initializing a symbolic simulation relation for symbolic model checking with a reasonable degree of precision and particularity. The specification further discloses (p. 19 lines 5-14) that:

and further discloses (see, p. 19, line 17 through p 20, line 4; Fig 3b) that:

and further discloses (p. 21, lines 15-16; Fig 6b, 621) that:

Appellant respectfully submits that at least in light of the above disclosure set forth by the specification, the claims set out and circumscribe initializing a symbolic simulation relation for an assertion graph configurable to express a justification property with a reasonable degree of precision and particularity.

The Examiner respectfully traverses Appellant's argument, the current claim language is disjoint and fails link how the Assertion graph is generated and how the generated Assertion graph is related to the circuit design, Appellants' specification clearly teaches the relationship between the Assertion Graph and the Circuit design, page 34 lines 10-15, disclose,

An assertion graph can be specified in an assertion graph language manually but with a assertion graph language as disclosed, it can also be derived automatically from a high level description, for example, from a register transfer language (RTL) description. Using such an assertion graph language, an assertion graph can be derived directly from a circuit description. Both methods for automatically deriving assertion graphs are potentially useful.

And, lines 20-23 of page 34 disclose,

A more typical scenario, though, would be to automatically generate the assertion graph from an RTL description and then to drive the equivalence verification of the RTL description and the circuit description through circuit simulation as previously described.

The Examiner is not permitted to read limitations, *or essential method steps* into the claims themselves, according to the current claim language the *assertion graph*, suddenly appears and there is no linkage between the claimed *circuit design* and the claimed *assertion graph*, therefore the claimed method, as currently claimed would *fail* to perform any verification of the claimed *circuit design.*

On pages 14 of the Appeal Brief, Appellants further argued;

The specification also discloses that (p. 16, lines 18-21) that:

The assertion graph can be seen as a monitor of the circuit, which can change over time. The circuit is simulated and results of the simulation are verified against the consequences in the assertion graph. The antecedent sequence on a path selects which traces to verify against the consequences.

The Examiner respectfully traverses the Appellant's argument, the claims do not have any language which teaches that the assertion graph is monitoring the circuit, and the circuit itself is not disclosed in the claims as well. The claims only teach a *circuit design* which is different from the *circuit* itself. Appellants' are attempting to read essential steps into the claims that do not exist.

On pages 14-15 of the Appeal Brief, Appellants further argued;

and further discloses (see p. 17, lines 13-14; Fig. 3a, 312-317) that:

For one embodiment, Figure 3a illustrates a method for computing the simulation relation for a model and an assertion graph.

and further discloses (p.21, lines 9-11; Fig. 6a, 612) that:

In block 612, a fixpoint simulation relation is computed using the antecedent strengthened assertion graph.

and further discloses (p. 21, lines 16-19; Fig. 6b, 622) that:

In block 622, a fixpoint simulation relation set for each edge e (denoted Sim*(e)) is computed using the strengthened antecedents computer for each edge in block 621.

Appellant respectfully submits that at least in light of the above disclosure set forth the specification, the claims set out and circumscribe, with a reasonable degree of precision and particularity, initializing a symbolic simulation relation for an assertion graph on a first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice domain is configurable to express a justification property to verify by computing the symbolic simulation relation.

Therefore appellant respectfully submits that when the claim is read in light of the specification, one skilled in the art would understand what is claimed including the relation between circuit verification and manipulation/initialization of a symbolic simulation for an assertion graph in a first symbolic lattice domain.

The Examiner respectfully traverses Appellant's arguments, it is still unclear, even in view of the cited section of Appellant's specification, if the assertion graph is being generated from the *(behavioral)* description of the circuit or if it is from the RTL description of the circuit.

On pages 15 and 16 of the Appeal Brief Appellant's further argue:

With regard to whether the specification provides a definition of the instant term "other finite state system", appellant respectfully submits that the specification discloses that (p. 7, lines 12-18; emphasis added) that:

Intuitively, a model of a circuit or other finite state system can be simulated and the behavior of the model can be verified against properties expressed in an assertion graph language. Formal semantics of the assertion graph language explain how to determine if the model satisfies the property or properties expressed by the assertion graph. Two important characteristics of this type of verification system are the expressiveness of the assertion graph language and the computational efficiency of carrying out the verification.

And further discloses (p. 7, lines 19-23 emphasis added) that:

For one embodiment, a finite state system can be formally defined on a nonempty finite set of states, S, as a nonempty transition relation, M, where (s1, s2) is an element of the transition relation, M, if there exists a transition in the finite state system from state s1 to state s2 and both s1 and s2 are elements of S. M is called a model of the finite state system.

Thus the specification clearly does provide a definition of the instant term, such that when the claim is read in light of the specification, one skilled in the art would understand what is claimed including the term "other finite state system."

The Examiner has found Appellants' arguments to be persuasive. It is clear exactly what are the metes and bounds of "M" are regarding the model of a *finite state system.* According to Appellants' arguments a *finite state system* is defined as a set of nonempty set of states, S, as a nonempty transition relation, where (S1, S2) is an element of the transition relation, M. Therefore it is clear that a *finite state system* as defined and argued by Appellant is a scientific principle divorced from any tangible structure and is therefore defined as a judicial exception under 35 U.S.C. 101 as being non-statutory subject matter.

On pages 17-19 Appellant's argued various sections of the specification, more specifically, page 16 lines 22 to page 17, line 12) which specifically discloses,

> For one embodiment, a simulation relation sequence can be defined for model checking according to the strong satisfiability criteria defined above. For an assertion graph G and a model M=(Pre, Post), define a simulation relation sequence, Sim_n: E→P(S), mapping edges between vertices in G into state subsets in M as follows:

The Examiner respectfully traverses Appellants' arguments, the current claim language fails to disclose the use of the term *model*, and Appellant's are attempting to argue limitations that are not in claim language itself. The Examiner cannot read limitations from the specification into the claims and must apply a reasonable and broad interpretation of the claim language, see section 2111 of the MPEP, "CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE INTERPRETATION" further, the Examiner is not permitted to read additional, essential, method steps into the claims, see MPEP 2111, more specifically,

In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (Claim 9 was directed to a process of analyzing data generated by mass spectrographic analysis of a gas. The process comprised selecting the data to be analyzed by subjecting the data to a mathematical manipulation. The examiner made rejections under 35 U.S.C. 101 and 102. In the 35 U.S.C. 102 rejection, the examiner explained that the claim was anticipated by a mental process augmented

by pencil and paper markings. The court agreed that the claim was not limited to using a machine to carry out the process since the claim did not explicitly set forth the machine. The court explained that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim,' to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The court found that applicant was advocating the latter, i.e., the impermissible importation of subject matter from the specification into the claim.).

Applicant's claim language has no express basis for *model checking to satisfy a defined criteria*.

On pages 18 and 19 Appellant's further argued;

> It will also be appreciated that there is a direct correspondence between the formal definition of $Sim_{sn}(y, y')$ and the iterated computing performed by BOX 1215 of Figure 12a. Appellant respectfully submits that at least in light of the above disclosure set forth by the specification, the claims set out and circumscribe computing the symbolic simulation relation for the assertion graph on the first symbolic lattice domain with a reasonable degree of precision and particularity.
>
> As relied upon above with regard to claims 4, 8, 14, 16 and 28, the test for definiteness under 35 U.S.C. § 112 is whether those skilled in the art would understand what is claimed when the claim is read in light of the specification. *Orthokinetics, Inc., supra.*
>
> Appellant respectfully submits that in light of the specification, those skilled in the art would understand what is being claimed, including the relation between circuit verification and the claimed computing of the symbolic simulation relation for the assertion graph on the first symbolic lattice domain and checking of the symbolic simulation relation to verify a plurality of properties as set forth by claims 5, 15 and 18.

The Examiner respectfully traverses Appellant's arguments, the current claim, even in light of the specification fails to set forth the specific method step of *generating the assertion graph from an RTL description of the circuit* because, even though the specification describes this step as occurring, the specification is not definitive regarding this being the only method used to generate the plurality of assertion graphs.

One of the criteria, set forth in the MPEP section 2173.02 regarding Clarity and Precision also states that one of the criteria for determining the Definiteness of the claim language is: "The

claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made." The current claim language, even in light of the specification, fails to specifically set forth that the assertion graph is generated from just the RTL description of the circuit or from another description of the circuit set forth by the circuit design, for example, page 34 lines 17-20 of the specification disclose;

"...manually generating an assertion graph may be prone to errors, but two assertion graphs could be automatically generated, one from the RTL description and one from the circuit design and the two assertion graphs can be checked for equivalency...",

The Examiner knows in the prior art there are teachings that disclose that assertion graphs are generated from the behavioral description of the circuit and then from the RTL description of the circuit and that the two will be compared to determine if the RTL description conforms to the behavioral description of the circuit, See U.S. Patent 6,163,876 Figures 1, 4 and 6 and the descriptive text. However, Appellant's specification is unclear regarding where the *second assertion graph* is generated from, therefore given the lack of description in the specification and the fact that the specification clearly teaches that two *assertion graphs* are being generated, there is a requirement that the *assertion graph* being claimed *clearly* and with *precision* disclose exactly from what portion of the circuit design, it is being created from.

Regarding Appellant's arguments regarding the 35 U.S.C. 101 rejections of claims 4, 5, 8, 14-18, 28 and 31-40, Appellant's have presented arguments in pages 20-28 of the Appeal brief, the Examiner will present responses as follows;

On page 21 Appellants' presented the following argument;

The Office Action of December 7, 2006 (p. 3 § 22) states that the manipulation of [symbolic simulation relations for an assertion graph and the subsequent verification of a symbolic simulation relation is merely teaching the manipulation of an abstract concept (citing MPEP § 2106.02, rev 5, 2006).

But, appellant respectfully notes that the cited section (§ 2106,02) refers to processes that simply manipulate abstract ideas without same claimed practical application, whereas all the instant claims set forth the practical application of performing formal verifications of circuits or other finite-state systems.

Appellant's then provide recitations of MPEP sections 2106.01

On page 22 Appellant's further argue;

The Office Action (p. 2-3, § 2.1) further states that although the specification discloses automated design verification for large scale integrated circuits, the claims include the term "other finite state system," so the claim language, even in light of the: specification, fails to disclose a useful result because the claimed invention could also be used to verify some abstract finite state system.

Appellant respectfully submits that the examiner is in error for reasoning that if the clamed invention could possibly be used to verify some abstract finite state system, then it can have no credible utility. Appellant submits that perhaps any patentable apparatus may have such a non-statutory use, which by itself would not be sufficient to establish patentability (use as landfill, for example) but a mere possibility of the existence of such a non-statutory use is insufficient to negate an otherwise credible assertion of utility, for the apparatus in establishing it as statutory subject matter.

An analysis of the instant claims must be performed in order to make a determination of whether the subject matter is statutory. Such analysis should not occur in a vacuum but should correlate each claim element with corresponding structures, materials or acts set forth in the specification.

On page 23 Appellants' further argued;

Appellant respectfully submits that the specification discloses (p. 7, lines 12-18; emphasis added) that:

...a circuit or other finite system can be simulated and the behavior of the model can be verified against properties expressed in an assertion graph language.

and further discloses (p. 7 lines 19-23; emphasis added) that:

For one embodiment, a finite state system can be formally defined on a nonempty finite set of states, S, as a nonempty transition relation, M, where (s1, s2) is an element of the transition relation, M, if there exists a transition in the finite state system from state s1 to state s2 and both s1 and s2 are elements of S. M is called a model of the finite state system.

Thus the specification clearly does provide a definition of the instant term, such that when the claim is read in light of the specification, one skilled in the art would understand what is claimed including the term "other finite state system."

The Examiner respectfully traverses Appellant's arguments, based on the arguments and the definition of the instant phrase *other finite state system* clearly the claimed subject matter is directed towards a scientific principle that is divorced from any tangible structure and is therefore defined as a judicial exception under 35 U.S.C. 101 as being non-statutory subject matter. The claimed *other finite system* is a set of state equations and is therefore manipulation of an abstract idea, MPEP section 2106.02 "Mathematical Algorithms", "If the "acts" of a claimed process manipulate only numbers, abstract concepts or ideas, or signals representing any of the foregoing, the acts are not being applied to appropriate subject matter."

Appellant's further argued on page 22;

Appellant respectfully submits that the examiner is in error for reasoning that if the claimed invention could possibly be used to verify some abstract finite state system, then it can have no credible utility, Appellant submits that perhaps any patentable apparatus may have such a non-statutory use, which by itself would not be sufficient to establish patentability (use as landfill, for example) but a mere possibility of the existence of such a non-statutory, use is insufficient to negate an otherwise credible assertion of utility for the apparatus in establishing it as statutory subject matter.

The Examiner respectfully points out that Appellant's claims are being rejected for being directed towards non-statutory subject matter and not being rejected for a lack of patentable utility.

Appellant's further argued on page 22;

An analysis of the instant claims must be performed in order to make: a determination of whether the subject matter is statutory, Such analysis should not occur in a vacuum but should correlate each claim element with corresponding structures, materials or acts set forth in the specification.

The Examiner has performed the analysis of Appellant's claimed regarding statutory subject matter in light of the specification and has found Appellant's claims to be directed towards abstract mathematical constructs which are non-statutory subject matter.

Appellants' argued on page 23 of the Appeal Brief that;

Thus the specification provides a definition of a finite state system, such that the claimed subject matter would be understood by a person of ordinary skill in the art of formal verification in the context of the entire patent.

The Federal Circuit makes it clear that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. "The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification" *Phillips v. AWH Corp.*, 415 F.3d at 1313.

Appellants' argue further on page 24 of the Appeal Brief that;

Therefore the specification provides a specific, substantial, and credible assertion of a well-established utility such that a person of ordinary skill in the art would appreciate why the invention is useful based on the characteristics of the invention (e.g., the technique is suitable for automated verification of more generalized properties in complex circuitry, protocols and software systems [i.e. or other finite state systems] with very large state spaces.

There is no support in Appellants' specification for protocols or software systems, further the claims are not directed towards statutory subject matter, they are directed towards other finite state systems, which according to Appellant's arguments and the specification are defined to be a set of state equations, which are mathematical abstract constructs. Appellant's claims have utility, they are however, not statutory.

Appellant's further argued on page 25 of the Appeal Brief;

The Supreme Court held that the focus in any statutory subject matter analysis be on the claim as a whole, stating "When a claim containing a mathematical formula implements or applies that formula in a structure or process which, when considered as a whole, is performing a function which the patent laws were designed to protect (e.g., transforming or reducing an article to a different state or thing, then the claim satisfies the requirements of § 101."

Appellant's claims are not transforming or reducing an article to a different state or thing, they are manipulating a simulation relation and then they are verifying an *other finite state system* by computing a simulation relation. This collection of method steps is, verifying a mathematical/theoretical construct, which is not an article.

Appellant's Further argued on page 25 of the Appeal Brief that;

> The Federal Circuit has pointed out (emphasis provided by the Fed. Cir.) that, "It is thus not necessary to determine whether a claim contains, as merely a part of the whole, any mathematical subject matter which standing alone would not be entitled to patent protection. Indeed, because the dispositive inquiry is whether the claim as a whole is directed statutory matter, it is irrelevant that a claim may contain, as part of the whole, subject matter which would be patentable by itself." A claim drawn to subject matter otherwise statutory otherwise statutory does not become nonstatutory because it uses a mathematical formula, [mathematical equation, mathematical algorithm,] computer program or digital computer." *Id* at 1543-1544 (quoting *Diehr,* 450 U.S. at 187, 209 USPQ at 5).

The Examiner respectfully traverses Appellant's argument, the claim language reads, *a formal verification of a circuit or* <u>*other finite state system*</u> the alternative is being set forth and therefore must be given full weight in consideration of the status of the claim as being directed towards statutory subject matter, when verification of a *circuit* is performed then manipulation of an actual electronic design is taking place and the claims are directed towards statutory subject matter, however, when verification of a state equation is performed, then only manipulation of an abstraction is taking place, MPEP section 2106.02 "Mathematical Algorithms", "If the "acts" of a claimed process manipulate only numbers, abstract concepts or ideas, or signals representing any of the foregoing, the acts are not being applied to appropriate subject matter."

Regarding the Appellant's arguments presented in regards to claim 28 presented on pages 26-28, the Examiner has found these arguments in regards to the *means for* language drawing structural support from the specification as regards using a computer system and not just software modules to be persuasive and the 35 U.S.C. 101 rejections of claim 28 in regards to being directed to software only have been withdrawn.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Dwin McTaggart Craig

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Conferees:

Leo P. Picard (SPE)

Paul Rodriguez (SPE)

Dwin McTaggart Craig (Examiner)

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

(Examiner)